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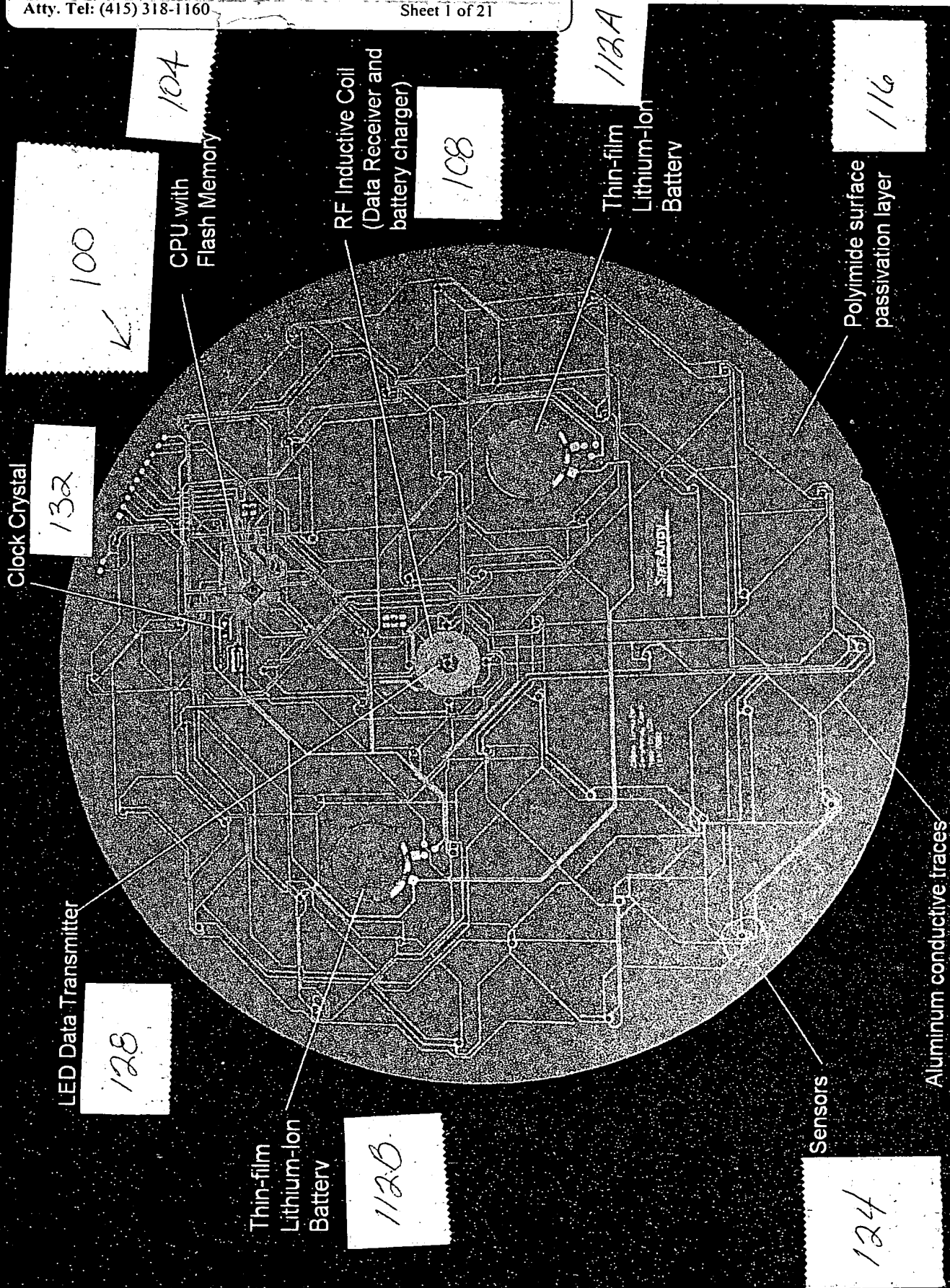


Fig. 1A

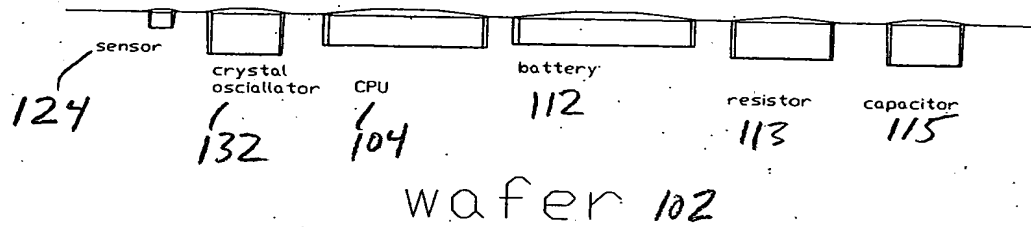


FIG. 1B

Components as imbedded in wafer (~~x-axis~~ not to scale)

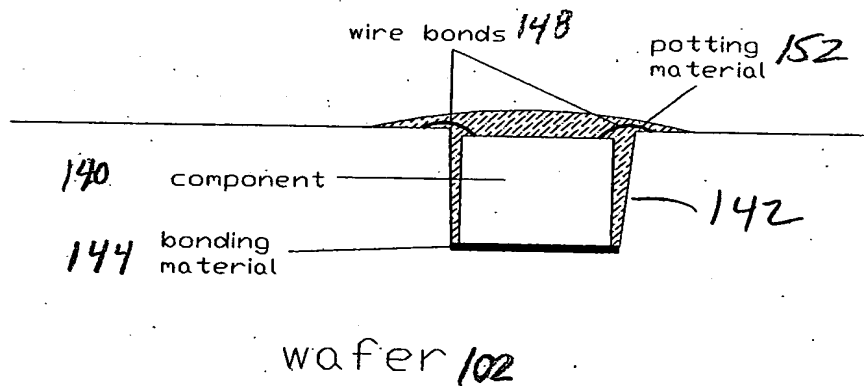


FIG. 1C

Detail of imbedded component (~~x-axis~~ not to scale)

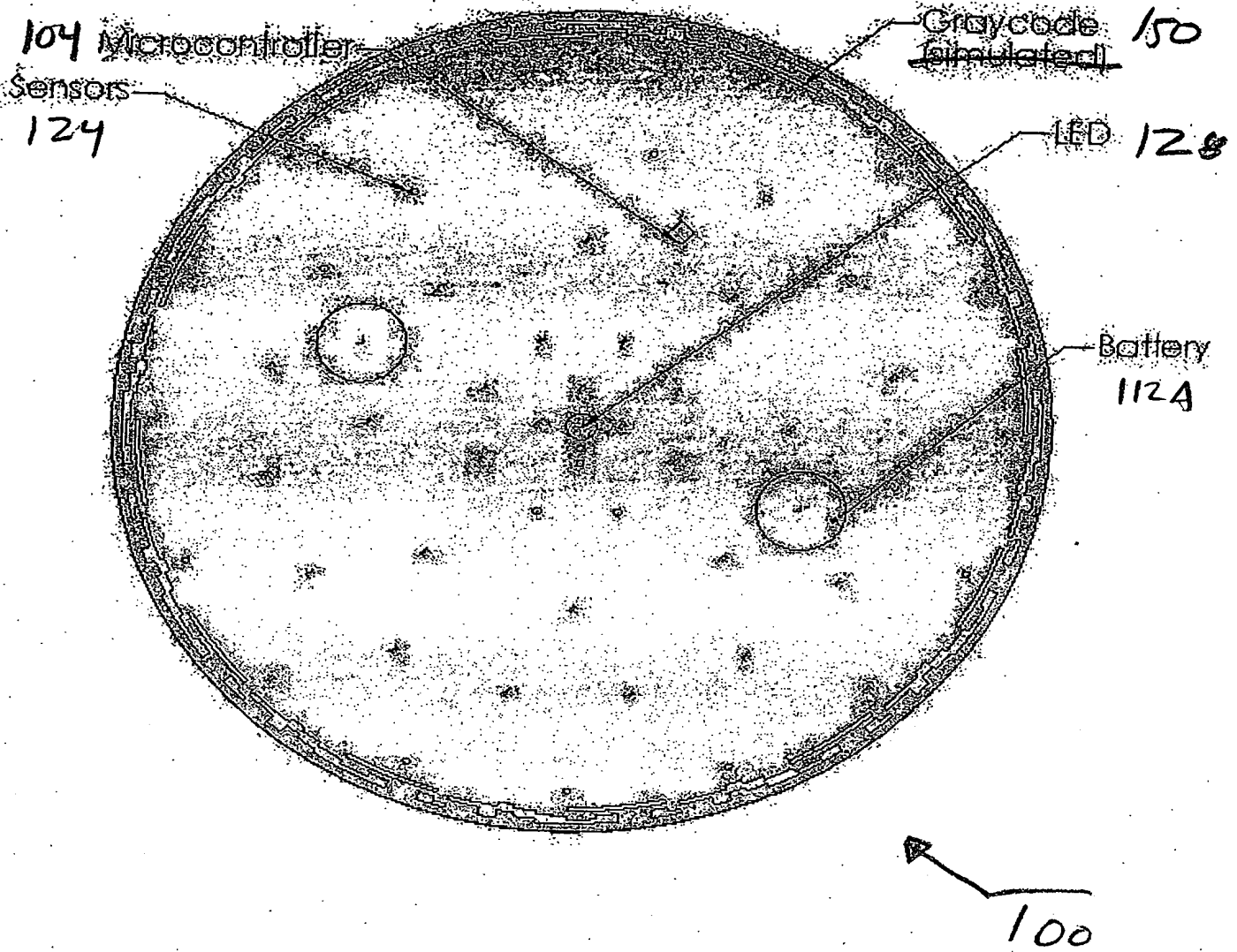


FIG 10

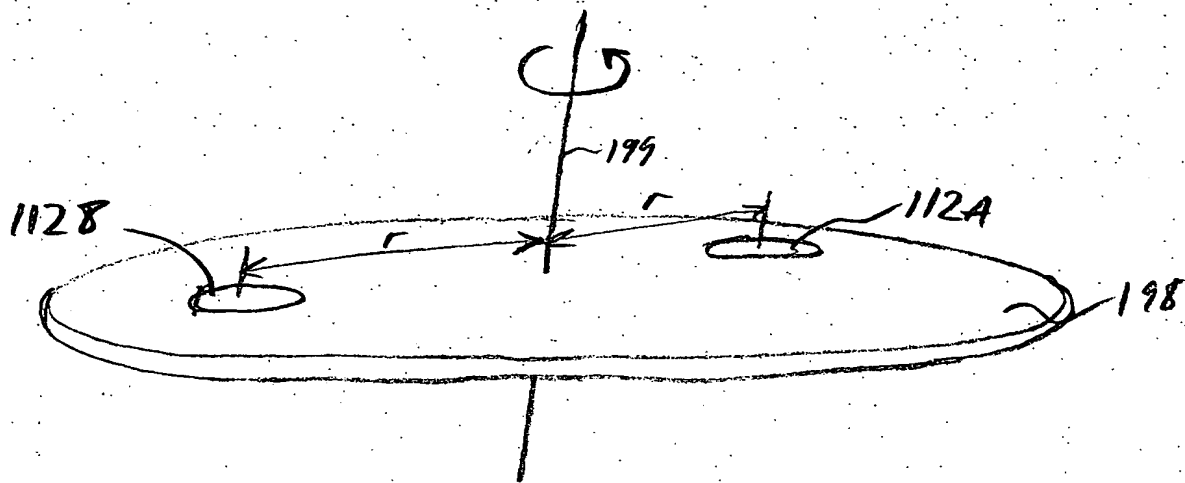


FIG. 1E

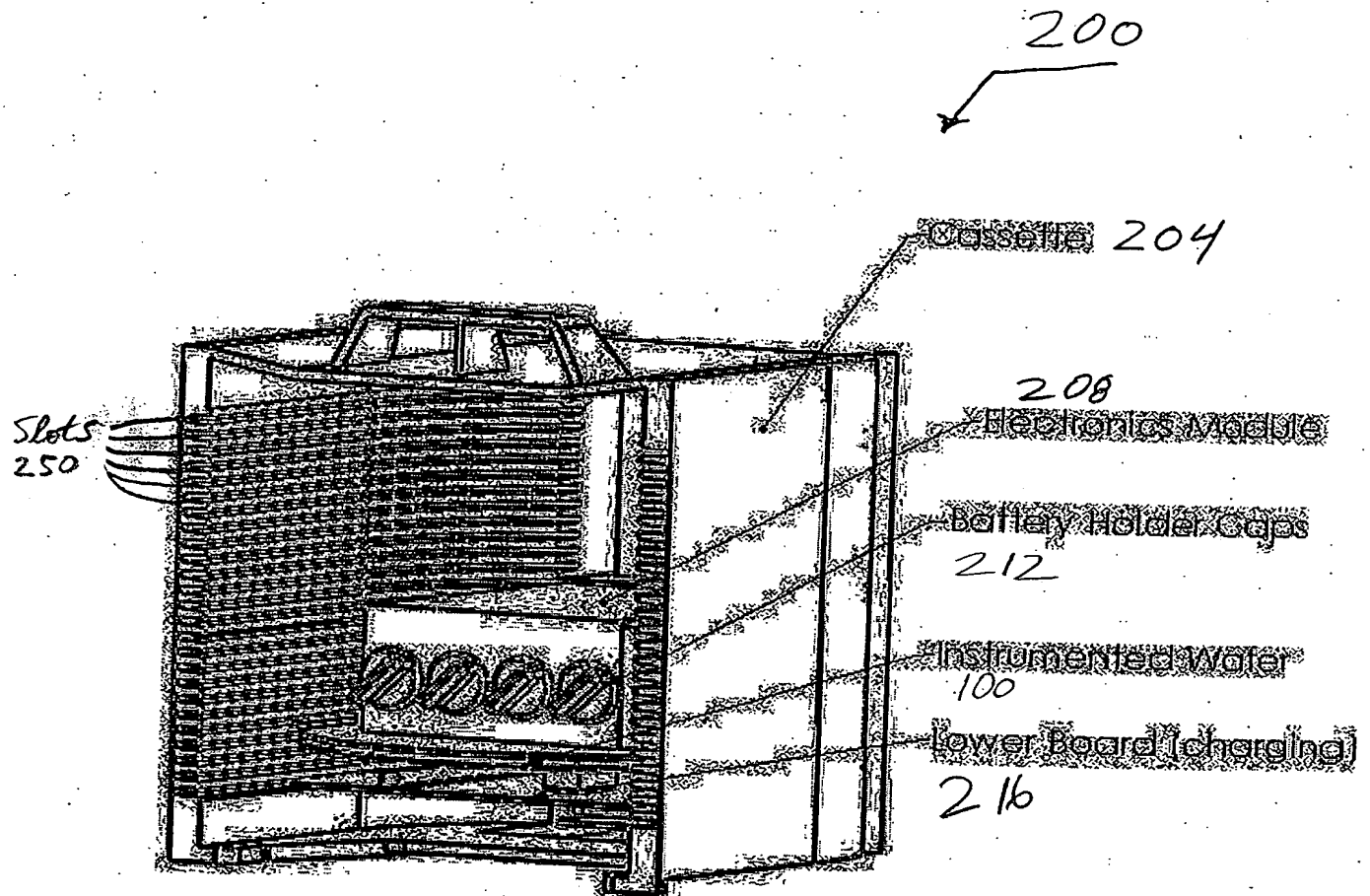


FIG. 2A

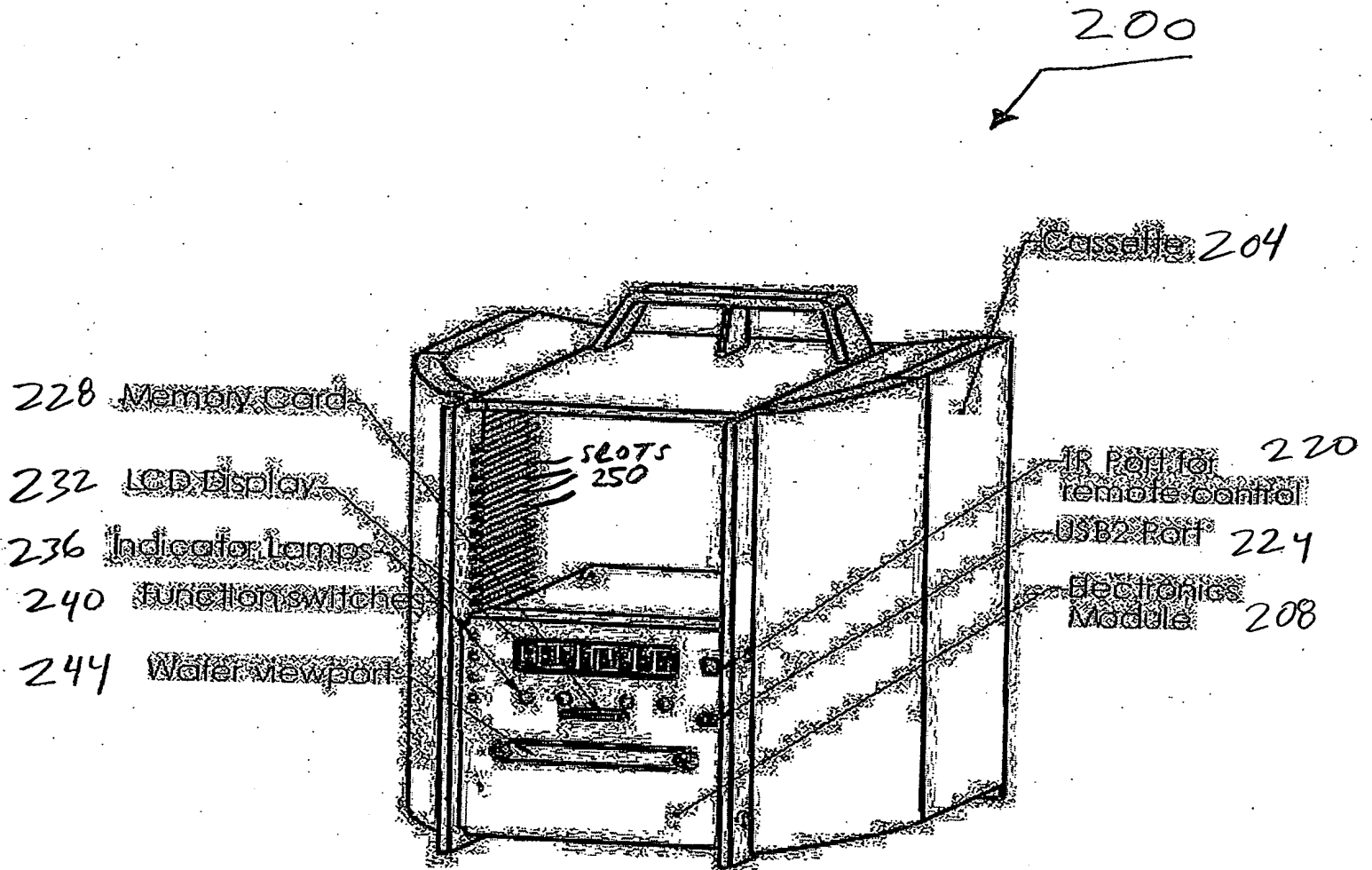


FIG. 2B

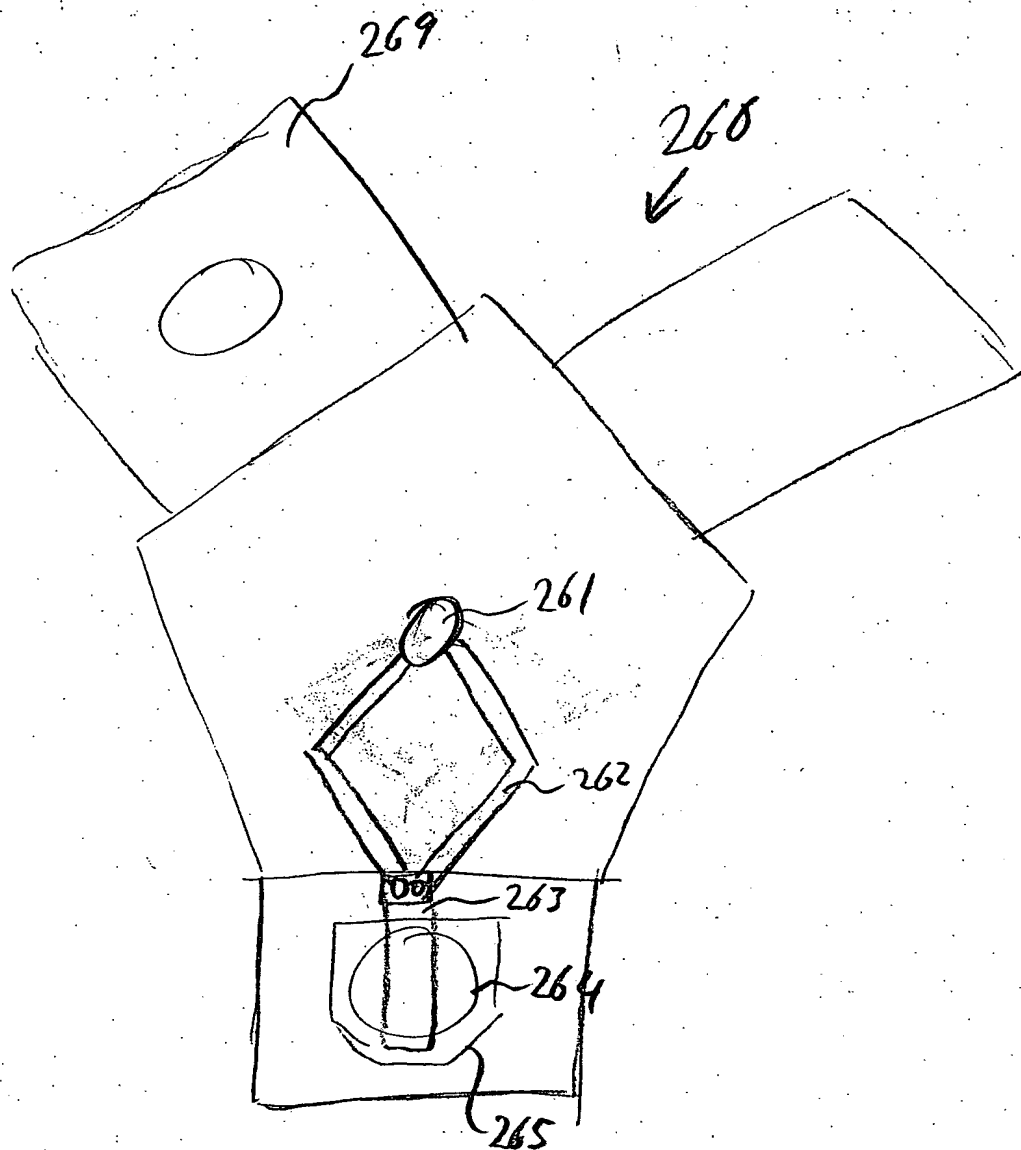
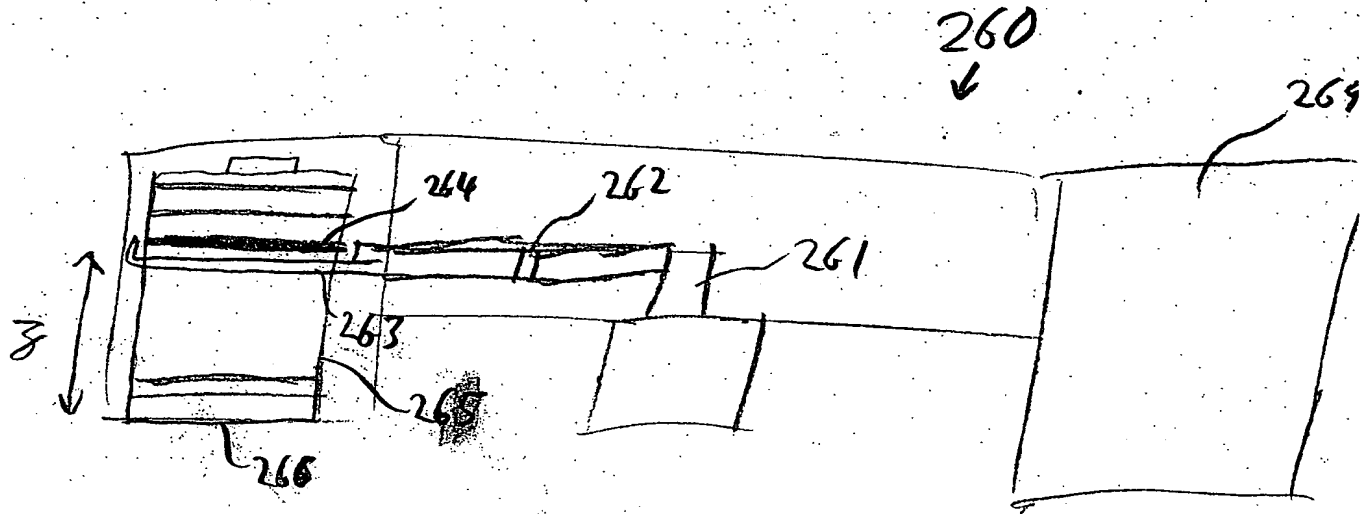
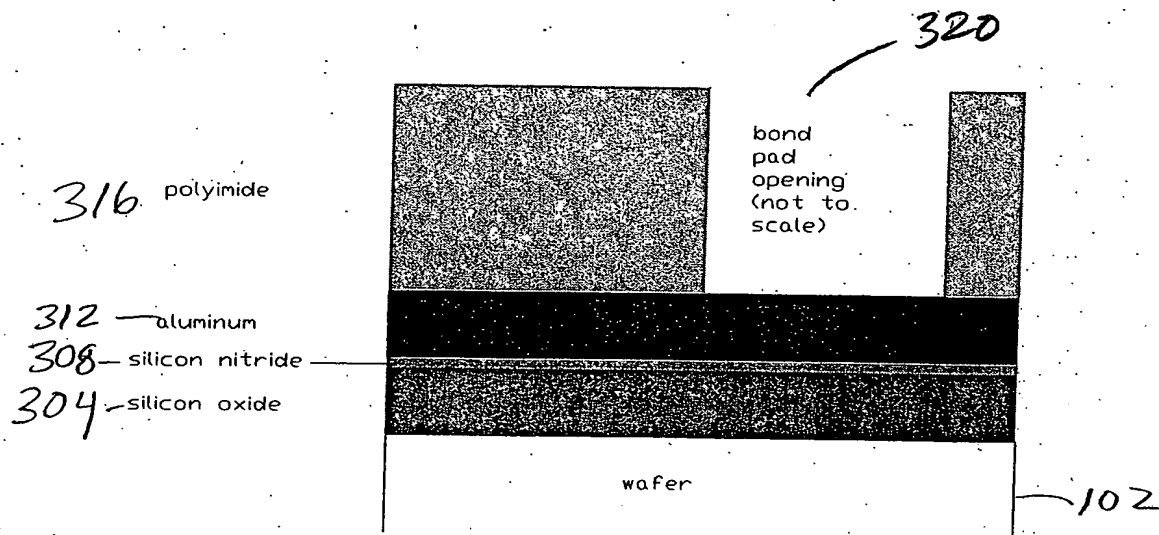


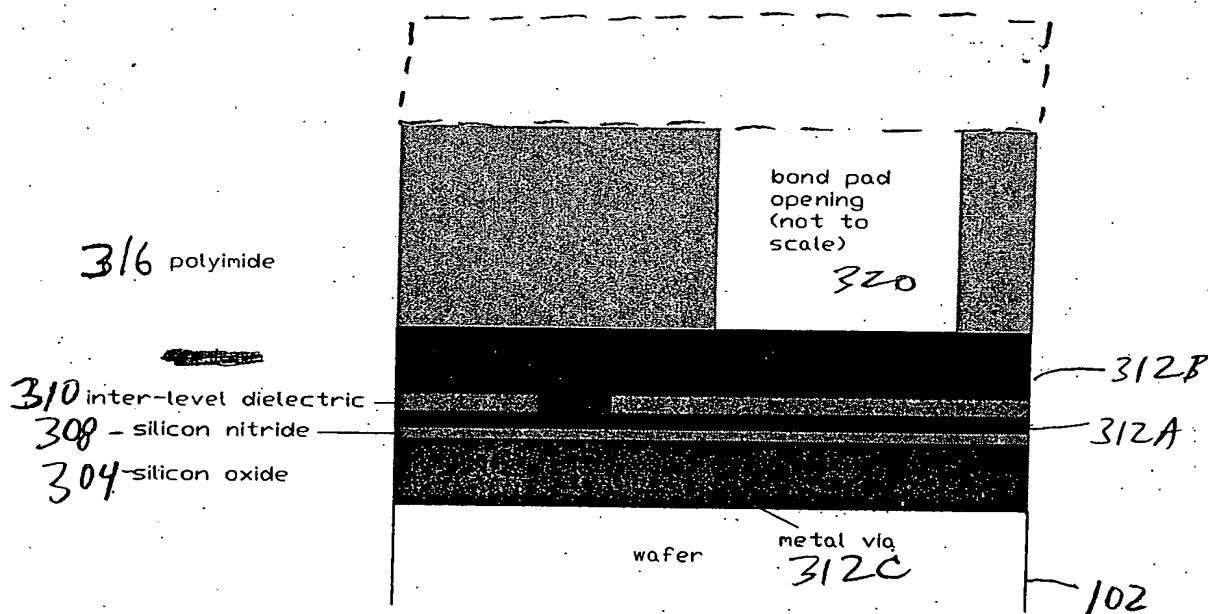
FIG 2C



2D



Single level metallization
 FIG. 3A



Double level metallization
 FIG. 3B

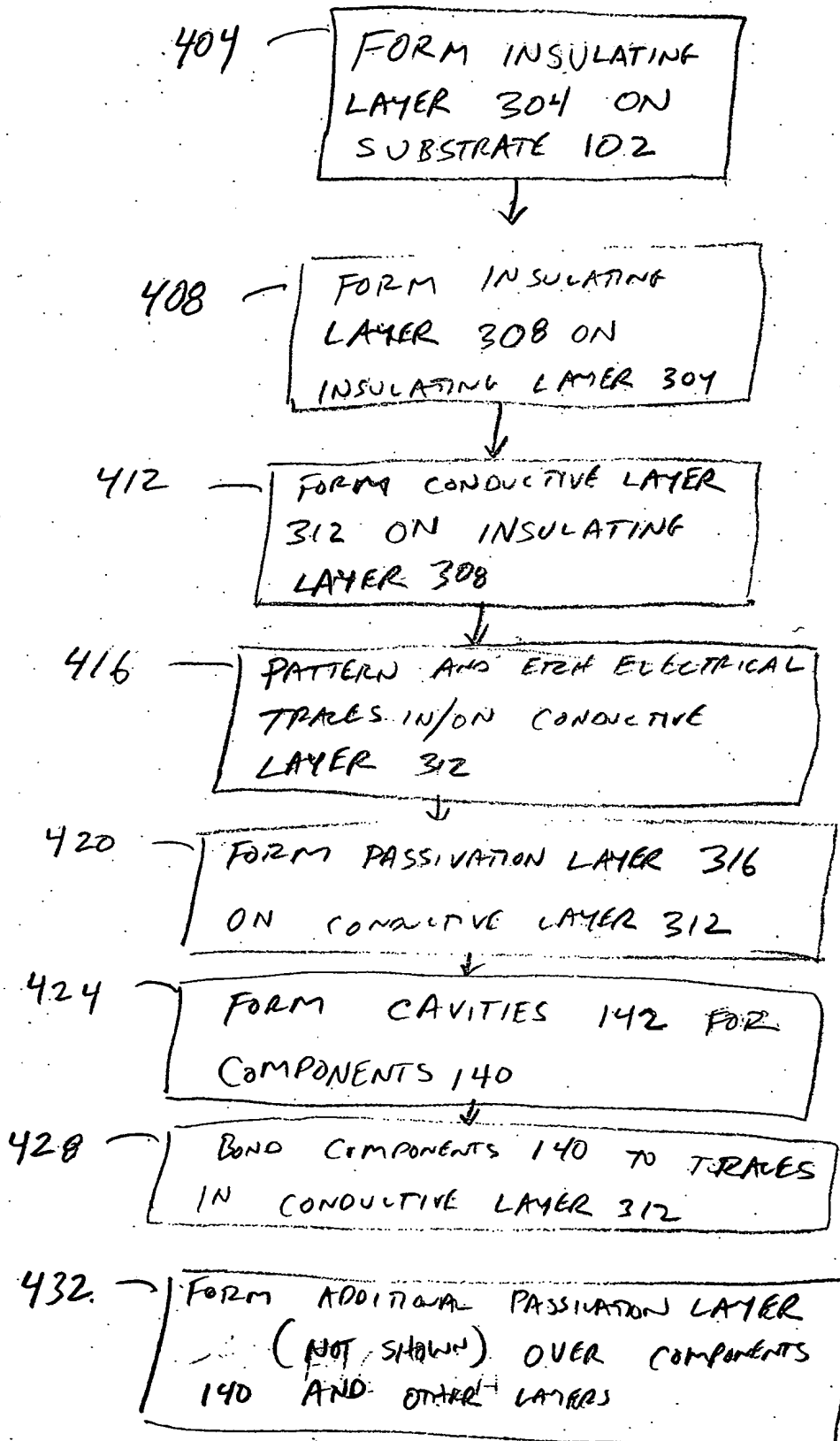


FIG 4A

404 — FORM INSULATING LAYER
304 ON SUBSTRATE 102

408 — FORM INSULATING LAYER
308 ON INSULATING LAYER
304

412 — FORM CONDUCTIVE LAYER
312A ON INSULATING LAYER
304

413 — FORM DIELECTRIC LAYER 310
ON CONDUCTIVE LAYER 312A

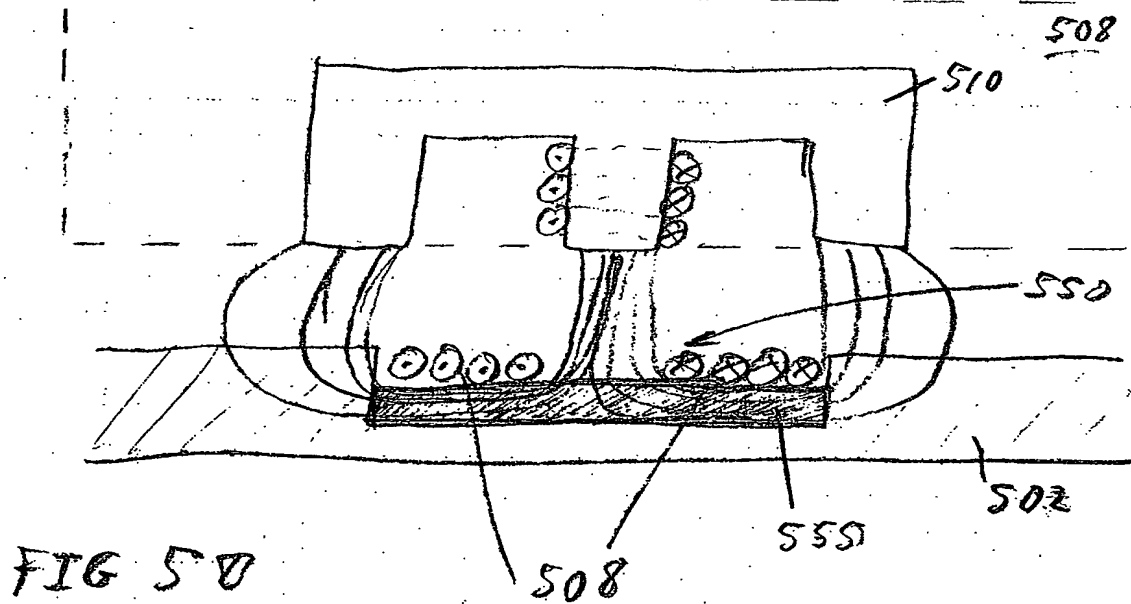
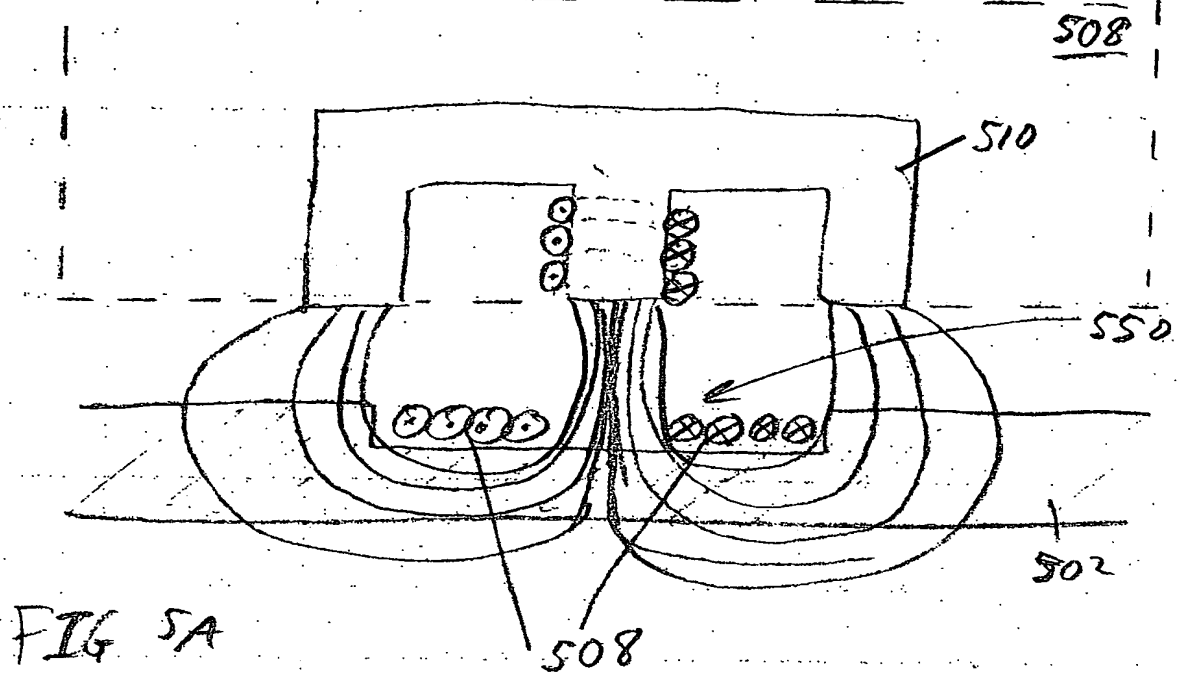
414 — FORM OPENING FOR VIAS 312C
IN DIELECTRIC LAYER 310

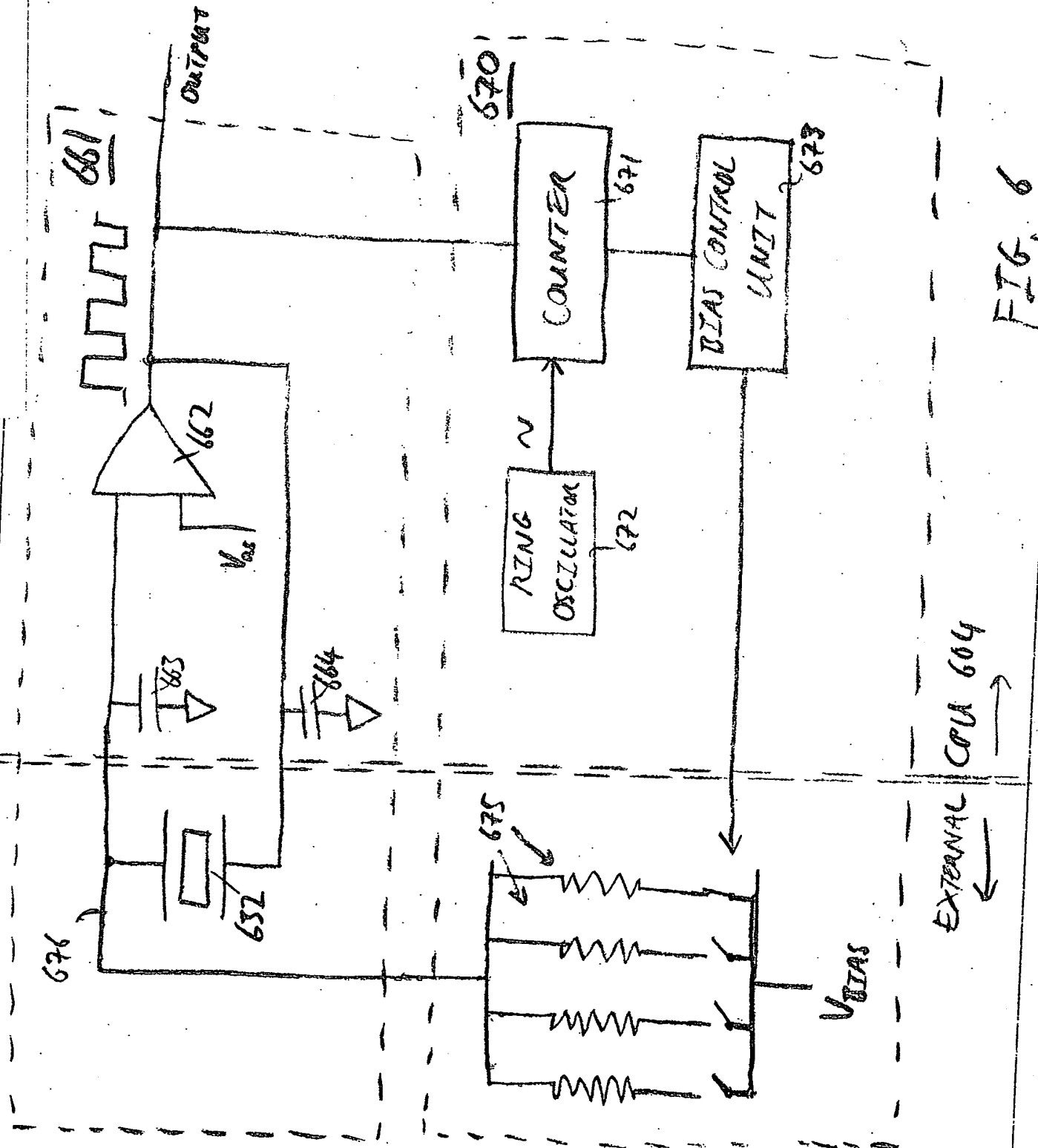
415 — FORM CONDUCTIVE LAYER 312B
AND VIAS 312C

416 — PATTERN AND ETCH ELECTRICAL TRACES
IN CONDUCTIVE LAYERS 312A,B

420 —
432 SAME AS IN
FIG 4A

436 — FORM ELECTRICAL AND CHEMICAL
PROTECTIVE SHIELD LAYER OVER
ADDITIONAL PASSIVATION LAYER
FIG 4B





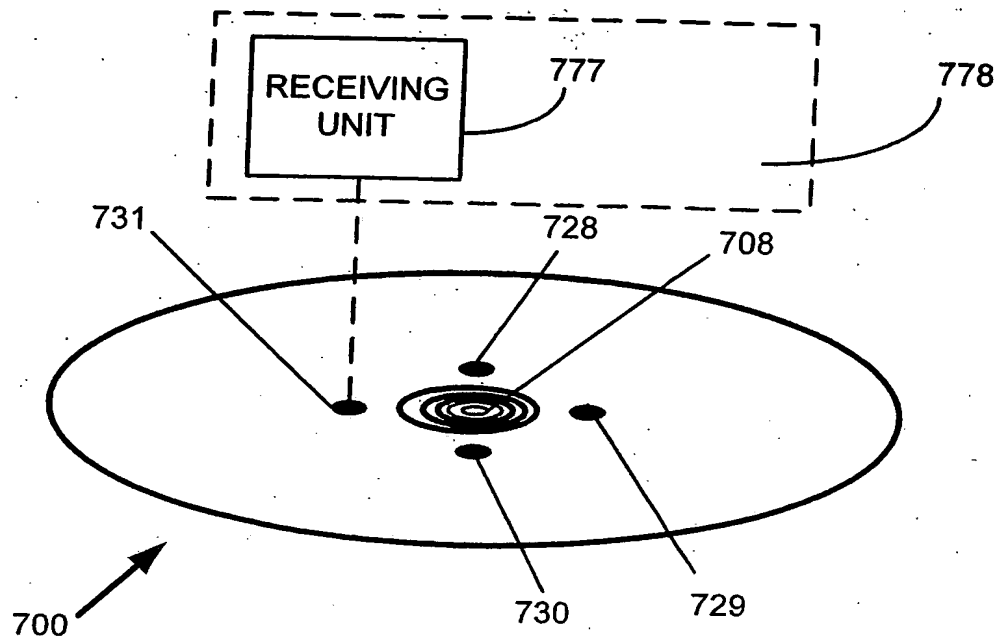


FIG. 7

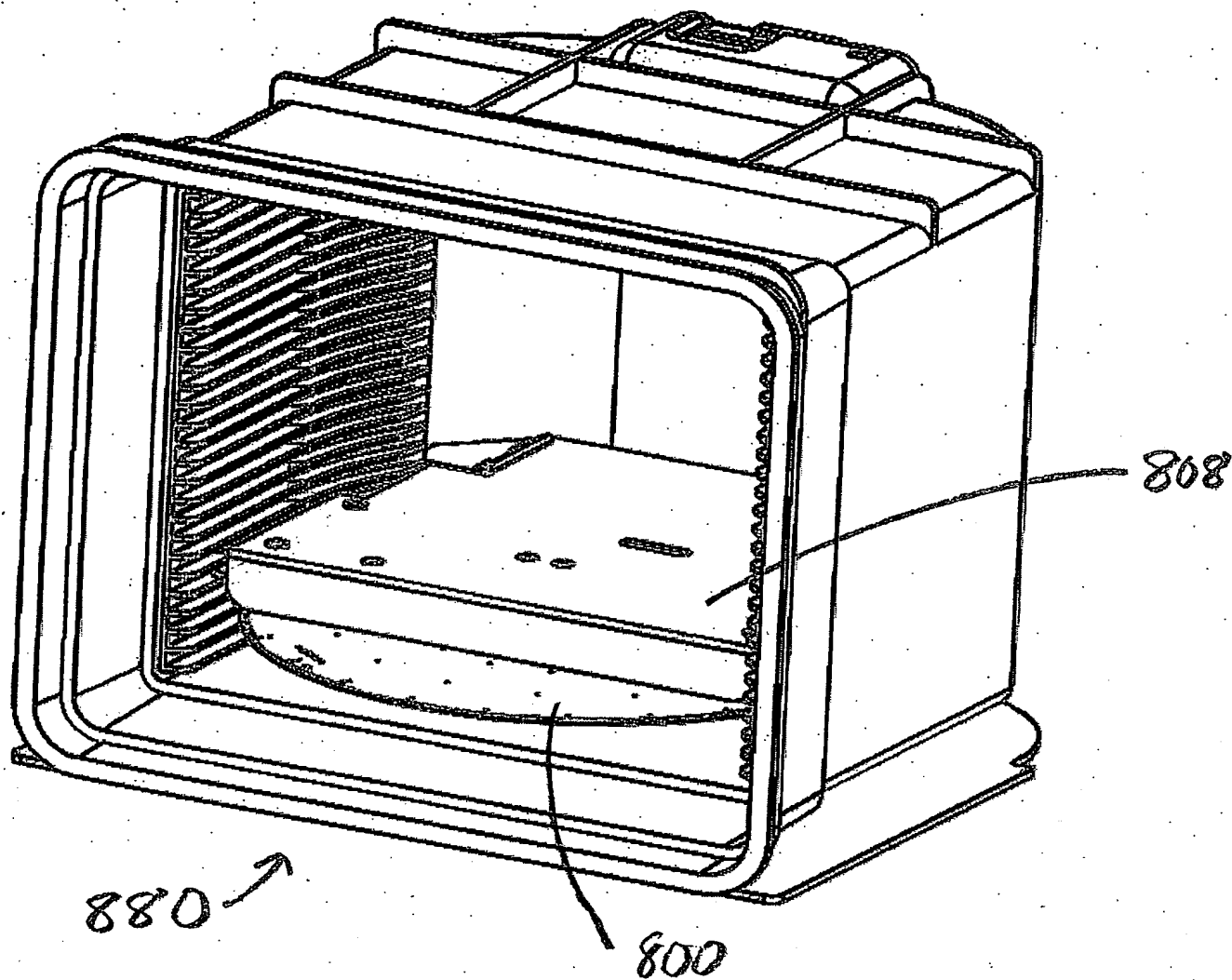


FIG 8A

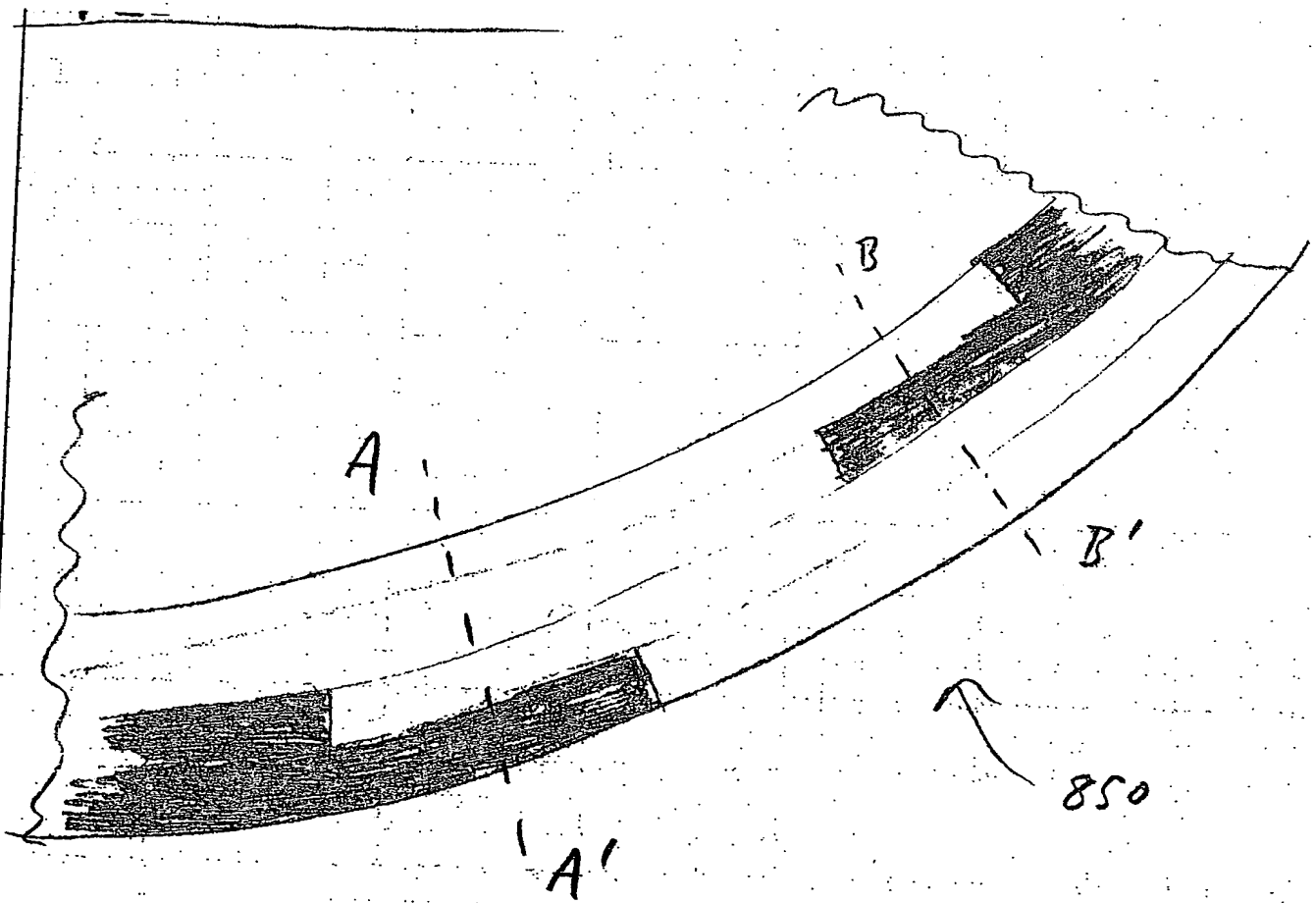


FIG 8B

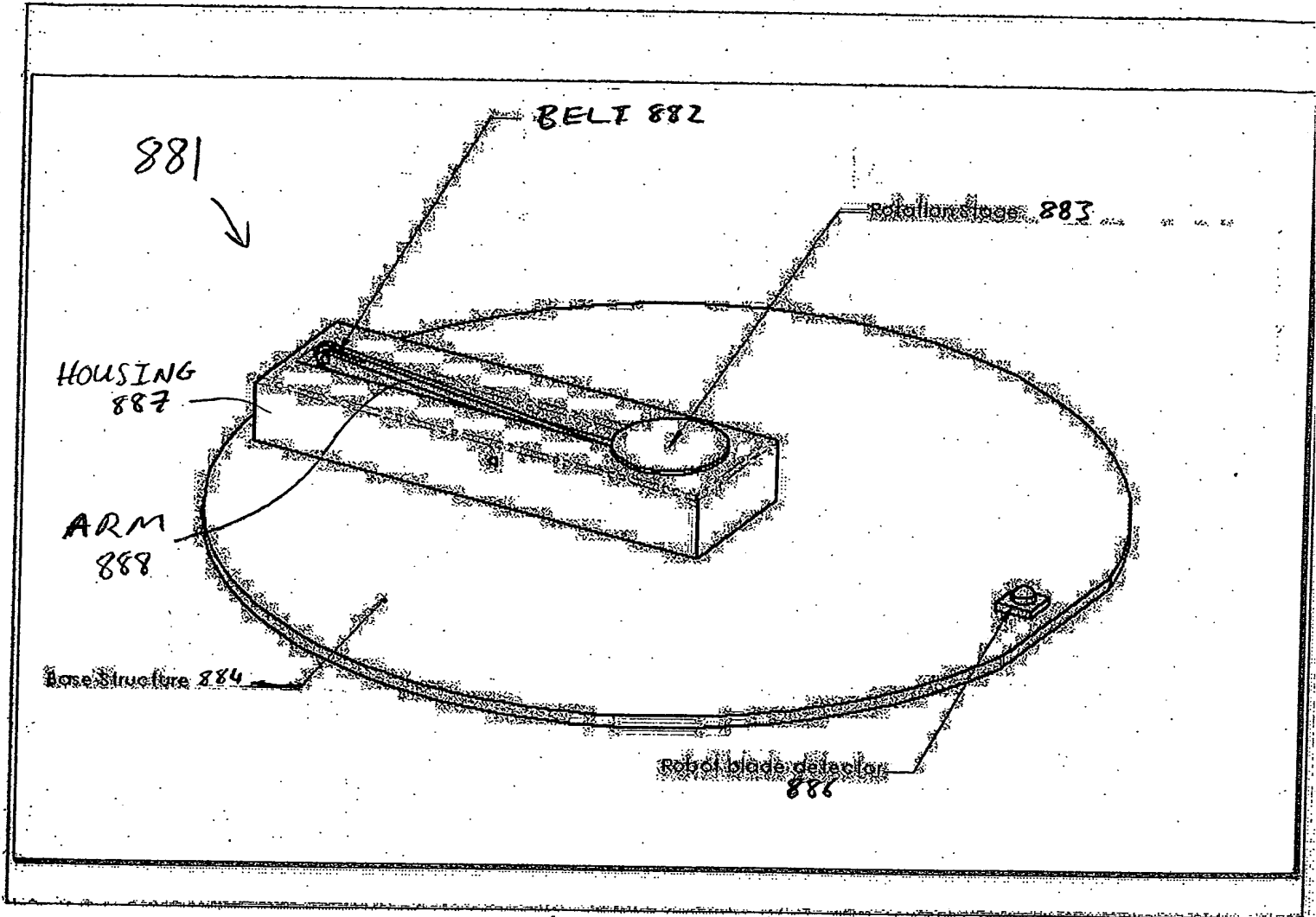
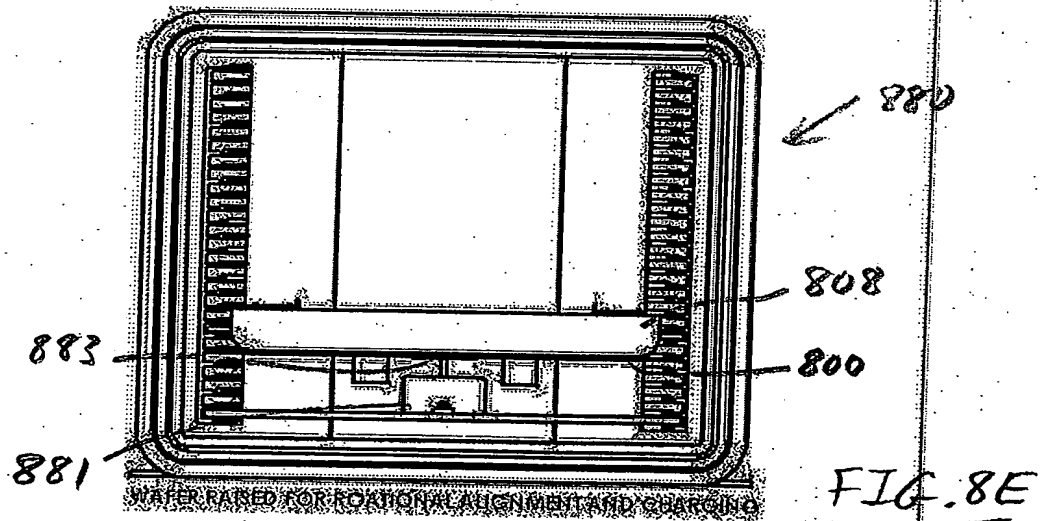
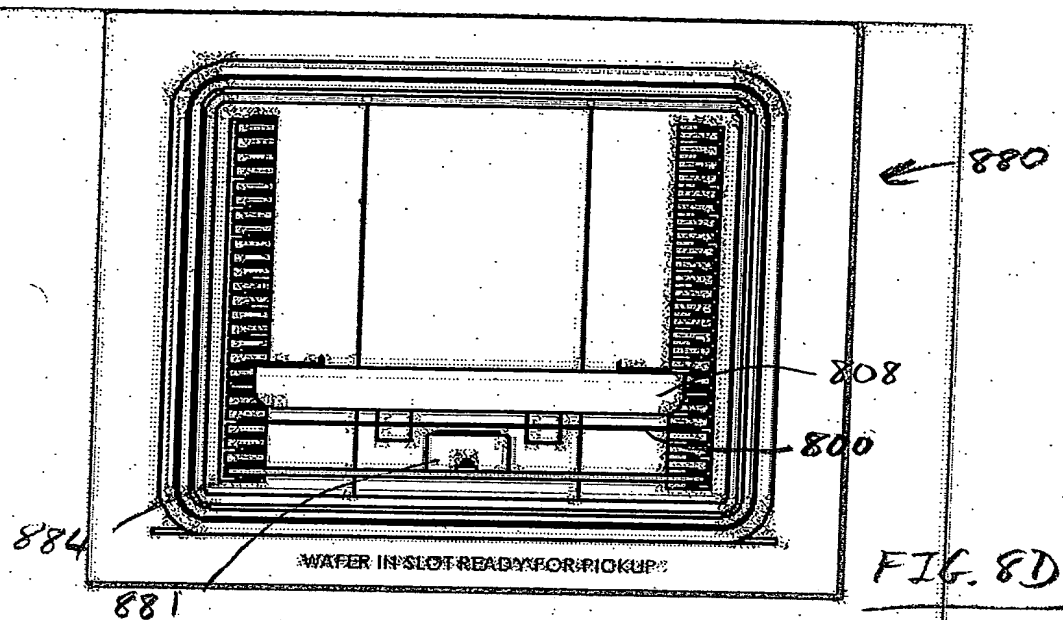


FIG 8C



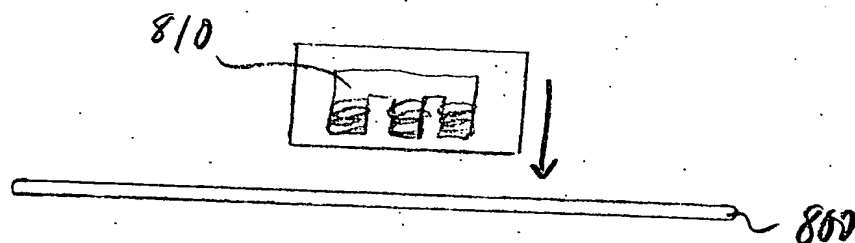
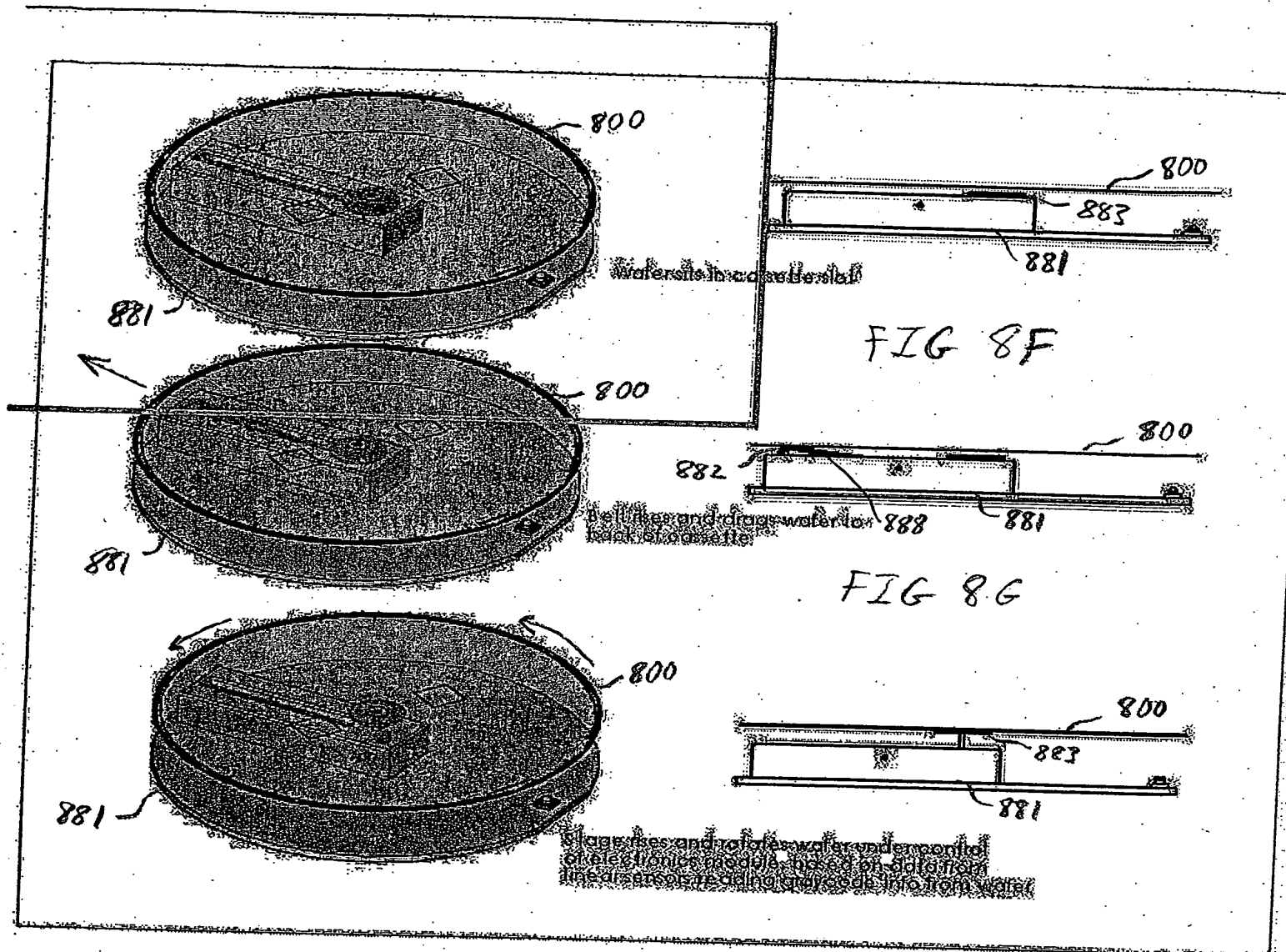


FIG 8I

22-141 60 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
CAMPAD

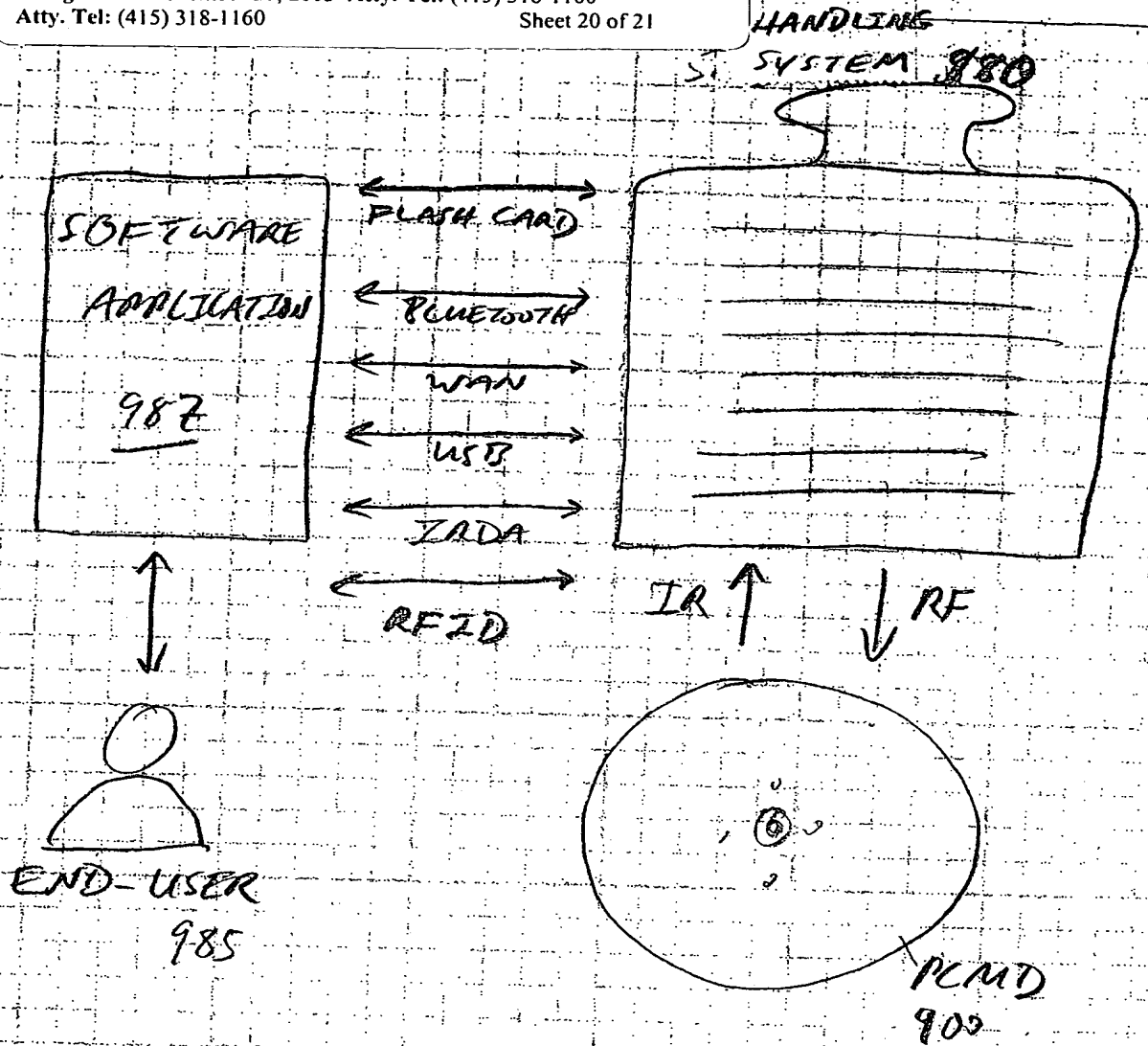


FIG 9

